REMARKS

A Petition for Extension of Time is being filed concurrently herewith.

Reconsideration and allowance in view of the foregoing amendments and the following remarks are respectfully requested.

Claims 1 and 5 have been amended, and new claims 10-14 have been added. Claims 1-14 are pending in this application.

Claims 1 and 4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Kenney. Applicant traverses the rejection for the following reasons.

Applicant submits that the remarks submitted on August 7, 2002 and April 29, 2002 are incorporated herein.

In addition to the arguments submitted in the previous Responses, Applicant submits that Yeh and Kenney, either alone or in combination, further fail to dislcose or even suggest a first active area, which incorporates a gate of a depletion mode transistor and operates as a bit line, as recited in claim 1, as amended. In other words, the bit line is formed by the first active area of each cell without adding an additional layer.

In contrast, the active area 16 of the Examiner's primary reference Yeh, which is pointed out by the Examiner, does not operate as a bit line. Fig. 5 of Yeh indicates that the layer 16 does not incorporate any gate of any transistor and does not operate as a bit line. The Examiner is cordially invited to point

out any passages or disclosure in Yeh, which describe or show the first active area which incorporates a gate of a depletion mode transistor and operates as a bit line. Applicant further submits that Kenney does not supply the above-noted deficiencies of Yeh.

Therefore, claim 1 and its dependent claim 4 are clearly patentable over Yeh in view of Kenney under 35 U.S.C. §103(a).

Claims 2, 3, 5-8 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Kenney, and further in view of Hoffman. Applicant traverses the rejection for the following reasons.

As set forth above, claim 1 is not made obvious over Yeh in view of Kenney. Applicant submits that Hoffman does not supply the above-noted deficiencies of Yeh and Kenney. Accordingly, it is believed that claims 2 and 3, which are dependent on claim 1, are patentable for the reasons discussed above with respect to claim 1, as well as on their own merits.

With respect to claim 5, all of the arguments in the previous response and in the paragraph set forth above with respect to claim 1 are applicable. Further, Applicant submits that Hoffman does not supply the above-noted deficiencies of Yeh and Kenney. Therefore, claim 5 and its dependent claims 6-9 are not made obvious over Yeh in view of Kenney, and further in view of Hoffman under 35 U.S.C. §103(a).

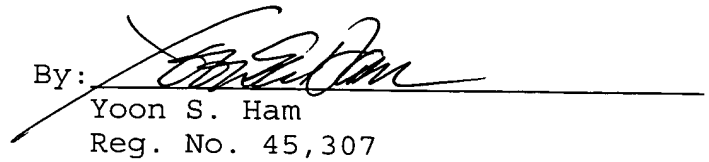
With respect to newly added claims 10-14, the prior art cited by the Examiner, at least, fail to disclose or suggest the first drain/source operated as a bit line, the word line and the cell plate of the claimed invention, as recited in claim 10.

Therefore, Applicant submits that claim 10 and its dependent claims 11-14 are patentable over Yeh, Kenney and Hoffman under 35 U.S.C. §103(a).

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "Version with Markings to Show Changes Made."

All objections and rejections having been addressed, it is respectfully submitted that claims 1-14 are now in condition for allowance and a notice to that effect is earnestly solicited. If any issues remain to be resolved, the Examiner is cordially invited to telephone the undersigned attorney at the number listed below.

Respectfully submitted,

By: 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1 and 5 as follows:

1. (Twice Amended) A ferroelectric memory cell for use in a ferroelectric random access memory (FeRAM) device, the ferroelectric memory cell comprising:

a first active area incorporating therein a gate of a depletion mode transistor and operating as a bit line;

a second active area adjacent to the first active area and incorporating therein a gate of an enhancement mode transistor;

a word line coupled to the gate of the depletion mode transistor and the gate of the enhancement mode transistor; and

a ferroelectric capacitor having first and second terminals, the first terminal coupled to a drain of the enhancement mode transistor and the second terminal coupled to a cell plate, for storing data.

5. (Twice Amended) A ferroelectric random access memory (FeRAM) device including a plurality of ferroelectric memory cells, comprising:

first active areas incorporating therein gates of depletion mode transistors and operating as bit lines;

second active areas adjacent to the first active areas incorporating therein gates of enhancement mode transistors;

word lines coupled to the gates of the depletion mode transistors and the gates of the enhancement mode transistors; and

ferroelectric capacitors each having first and second terminals, the first terminal coupled to a drain of a corresponding transistor of the enhancement mode transistors and the second terminal coupled to a common cell plate, for storing data.